Experimental Results in Evolutionary Fault-Recovery for Field Programmable Analog Devices

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Abstract

This paper presents experimental results of fast intrinsic evolutionary design and evolutionary fault recovery of a 4-bit Digital to Analog Converter (DAC) using the JPL stand-alone board-level evolvable system (SABLES). SABLES is part of an effort to achieve integrated evolvable systems and provides autonomous, fast (tens to hundreds of seconds), on-chip evolution involving about 100,000 circuit evaluations. Its main components are a JPL Field Programmable Transistor Array (FPTA) chip used as transistor-level reconfigurable hardware, and a TI DSP that implements the evolutionary algorithm controlling the FPTA reconfiguration. The paper describes an experiment consisting of the hierarchical evolution of a 4-bit DAC using 20 cells of the FPTA chip. Fault-recovery is demonstrated after applying stuck-at 0 faults to all switches of one particular cell, and using evolution to recover functionality. It has been verified that the functionality can be recovered in less than one minute after the fault is detected while the evolutionary design of the 4-bit DAC from scratch took about 3 minutes.

1. Introduction

Since the early days of the space program, spacecraft reliability has been steadily improving. Despite the technological progress, still until now expensive spacecraft have been lost or impaired by single events that escaped detection prior to launch. A failure in a spacecraft has to be treated in different way than failures in terrestrial systems. For terrestrial systems, engineers can often test devices to the point of failure to evaluate a design and when a failure occurs in service, components can be recovered and studied. In contrast, expensive spacecraft systems are rarely tested to failure. To analyze failures during a mission, engineers must rely on telemetry, ground-test data, and operational analysis. Moreover only rarely can components be recovered. From this limited historical information of failure data, four broad categories of spacecraft failures have been defined [1]: (1) events caused by the space environment, such as radiation damage to circuits (2) incidents for which some aspect of the design was inadequate while meeting the flight requirements; (3) problems with the quality of the spacecraft or of parts used in the design, or (4) a predetermined set of "other" failures, which include operational errors and unknown causes.

This work concentrates on the first category because design and environment causes continue to be the most significant sources of failure, in spite of the improvement in design techniques and the use of more refined environmental models. This work demonstrates that by using evolutionary techniques and an evolution oriented reconfigurable hardware (EORA) [2] we are able to design electronics circuit and recover from faults. After evolving the circuit to design a 4-bit DAC application, faults are simulated by constraining 75 reconfigurable switches of two FPTA cells to be opened. Once the fault is detected, evolutionary self-recovery is performed in real-time in less then a minute using the same reconfigurable hardware and without the need for fault-identification.

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The paper is divided as follows. Section 2 overviews the potential failure in spacecrafts due to the space environment and the classical fault-tolerant techniques. Section 3 describes the components of SABLES, including the FPTA2 chip and the DSP system. Section 4 describes the hierarchical evolution of a 4-bit DAC. Section 5 shows the evolutionary fault recovery experiments performed on the evolutionary synthesized 4-bit DAC. Section 6 concludes the work.

2. Failures caused by space environment

The space environment creates an assortment of hazards such as meteorite and orbital debris whose ill effects can range from degraded performance up to catastrophic loss of a spacecraft but remains less statistically significant than other environmental factors such as thermal and radiation effects. Variations in solar radiation (albedo) can lead to a dynamic spacecraft thermal environment, especially for small spacecrafts, which can drive temperatures at thermal junctions to critical limits. The radiation environment is perhaps the most significant in terms of spacecraft failures.

The radiation environment is characterized as containing energetic particles (ranging from 100KeV up to several GeV) that are either trapped by, or passing through, the earth's magnetosphere. The radiation can affect circuitry in different ways depending on the type of energy in the particle. The majority of occurrences involving radiation are single-event upsets, which cause a state change, such as a digit being "flipped" from zero state to a one. Such events are common and not of concern in most circumstances, since error detection and correction (EDAC) software can locate and reverse the event. Another type of event, of considerably greater concern is the single-event latchup (SEL), which causes a part to draw excessive current until it is shut down. SELs are serious, but cycling the power to a component will usually reset a circuit by eliminating the locally deposited charge which triggered parasitic bipolar transistors. Damage can result, however, since the SEL is effectively a short circuit. A third type of failure is the single-event burnout (SEB) which refers to not recoverable failures of power MOSFET transistors due to a high current state in a power transistor.

Failures do not necessarily place mission objectives in jeopardy if backup systems are available or if the spacecraft design is sufficiently flexible to allow workarounds. Historically, redundancy has been a central method of achieving resistance to failure. A 1994 JPL study of the critical telecommunication system on six prior missions (Voyager 1 and 2, Viking 1 and 2, Galileo, and Magellan) revealed that redundancy is likely to have saved five of these missions from catastrophic failure [3]. But redundancy is costly in terms of the resources that must be devoted to backup systems. Redundant systems add mass, consume power, require more wiring, and increase the dimensions of the software used to operate the spacecraft. Future spacecraft are likely to rely more heavily upon autonomous systems for fault detection, isolation and recovery as proposed in this paper for electronics circuits.

One of the goals of future electronics is to design radiation-immune electronic components [4]. More generally, the development of novel fault-tolerant methods for circuit design will benefit not only aerospace applications, but fields with extreme temperature and radiation environments. Our mission, therefore, is to design and develop electronic components and systems that are inherently insensitive to faults by using on-board evolution in hardware to achieve fault-tolerant and highly reliable systems. Evolutionary algorithms have been used with success for designing fault-tolerant systems in electronics [5]. Thompson and Layzell used the population effect of Evolutionary Algorithms (EA) to design fault-tolerant circuit [6,7]. More recently, Lohn showed how the EA can be applied to recover fault in digital reconfigurable device such as FPGA that are used routinely in current spacecraft [8]. Hounsell and Arslan investigated the ability of EA to adapt to increasing numbers of faults of a 31-tap low-pass FIR filter [9]. Finally Gwaltney and Ferguson applied the same technology to recover the functionality of analog controller of motor driver [10].

The next section presents our JPL stand-alone board-level evolvable system (SABLES) used as a testbed for electronic circuit evolution and recovery.

3. A stand-alone board-level evolvable system

SABLES integrates an FPTA and a DSP implementing the Evolutionary Platform (EP). The system is stand-alone and is connected to the PC only for the purpose of receiving specifications and communicating back the results of evolution for analysis.

The FPTA is an implementation of an evolution-oriented reconfigurable architecture (EORA) [2]. The latest FPTA chip consists of an 8x8 array of reconfigurable cells. Each cell has a transistor array as well as a set of other programmable resources, including programmable resistors and static capacitors. Figure 1 provides a detailed view of the reconfigurable transistor array cell. The reconfigurable circuitry consists of 14 transistors connected through 44 switches and is able to implement different building blocks for analog processing, such as two- and three-stage OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Details of the FPTA can be found in [11].

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The evolutionary algorithm was implemented in a DSP that directly controlled the FPTA, together forming a board-level evolvable system with fast internal communication ensured by a 32-bit bus operating at 7.5MHz. Details of the EP were presented in [12].

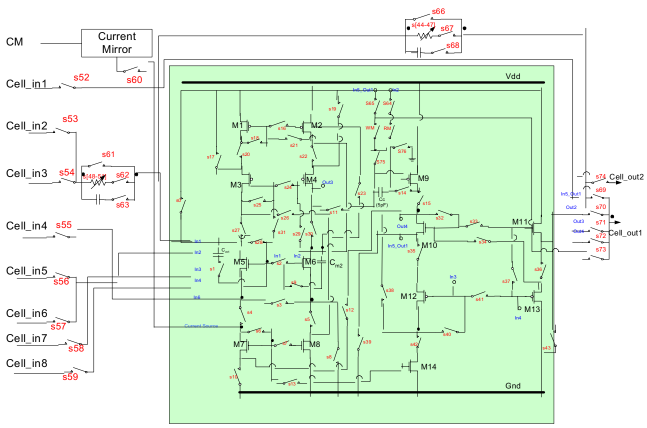

Figure 1 Schematic of cell transistor array .

4. Evolution of a 4-bit DAC

It has been shown that evolving a circuit of more than 20 transistors (4-bit DAC) in the FPTA using MOS transistor as building blocks is a difficult task [13]. The objective of our experiment was therefore to overcome this limitation and synthesize a 4-bit DAC hierarchically: evolving first a 2-bit DAC, using it as a building block to evolve a 3-bit DAC, and reusing it to evolve a 4-bit DAC. The rational of the methodology is based on reducing the search space by keeping an acceptable scope/focus and increasing the level of abstraction e.g. through the use of increasingly higher level building blocks. The method proposed is based upon encapsulation and design re-use and one example is the evolution of a 4-bit Digital to Analog Converter (DAC).

20 FPTA cells have been used in this experiment. Four cells were used to map a previously evolved 3-bit DAC. This 3-bit DAC was evolved using a previously evolved 2-bit DAC. Four other cells had their topologies constrained to human designed Operational Amplifier mapped onto the FPTA cells. It was verified in previous experiments [14] that the use of OpAmps improved the evolutionary performance for filter evolution. In the 4-bit DAC case we configure the four cells closer to the circuit output (Figure 2) as OpAmps, to achieve amplification and buffering effects. The remaining 12 cells have their switches' states controlled by evolution.

The FPTA output is read back and a total of 80 samples are used for fitness computation. The fitness evaluation starts by computing the average value of the circuit output O4 for the 16 different input configurations of the 4-bit DAC, (5 samples per input configuration). The resulting average vector is represented by Out_0, Out_1 until Out_{15}.

This fitness function evaluates the voltage differences' generated by the outputs (Out_1–Out_0, Out_2–Out_1, etc). The voltage difference values must be positive to achieve a monotonic output function and their range should be limited to improve the DAC linearity.

5. Fault Tolerance Experiments

In this experiment, we simulate faults due to radiation by using the stuck-at fault model. The fault is implemented by opening all the switches of two cells of the evolved 4-bit DAC mapping OpAmps. This is illustrated in Figure 2, where the faulty cells are filled in black. This kind of fault could be caused by a SEL event in a spacecraft, where the cell programming data bus is shorted to the ground bus. The four cells labeled '0', '1', '2' and '3' map the previously evolved 3-bit DAC, whose output is O3. This 3-bit DAC was evolved using a previously evolved 2-bit DAC (cells 0 and 1) whose output is O2. The two cells labeled 'A' have their topologies constrained to human designed Operational Amplifiers mapped onto the FPTA cells. The grey cells have their switches' states controlled by evolution. O4 is the output of the 4-bit DAC.

The two black cells were mapping human designed OpAmps before the fault was applied. They were selected for fault application because opening their switches caused larger response deterioration in the evolved DAC comparing to the other cells (Figure 4). It should also be pointed out however that we did not apply faults to the cells implementing the 3-bit converter building block. The recovery process would have been more difficult if the 3-bit building block functionality had been lost, since hierarchical evolution was a key factor for the 4-bit DAC synthesis.

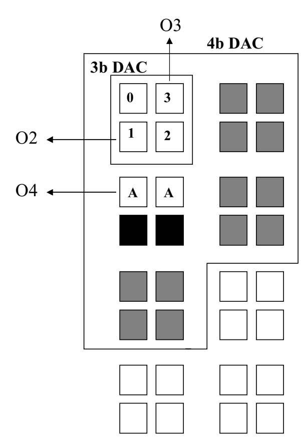

Figure 2. Topology employed for the 4-bit DAC evolutionary recovery. 20 cells actually used in the experiment involved by the 4b DAC line. Cells in black are the faulty cells.

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In the beginning of the experiment a fault-free 4-bit DAC was evolved. In this experiment we used a population size of 500 individuals and a total of 200 generations, lasting about 5 minutes. The circuit response is shown in Figure 3.

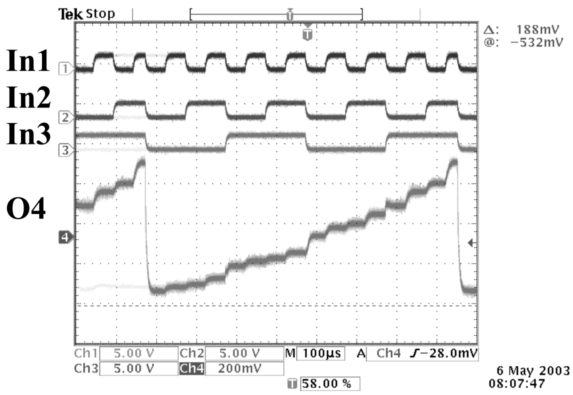

Figure 3. Evolved 4-bit DAC inputs (In1, In2 and In3) and output (O4). MSB (In4) not included due to limitation in the number of oscilloscope channels.

The next step of the experiment consisted of applying the faults to the two OpAmp cells of the evolved DAC. The deteriorated response of the faulty DAC is shown in Figure 4.

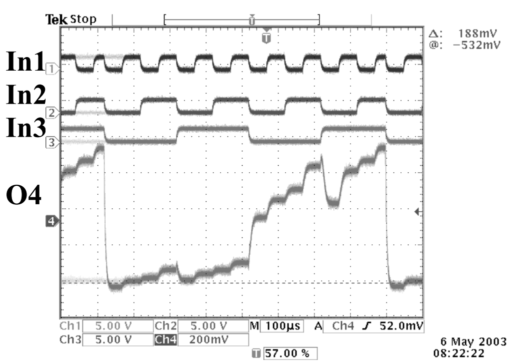

Figure 4. Evolved 4-bit DAC with two faulty cells.

Finally, we apply evolution to recover the circuit functionality. Again, only the switches in the grey cells had their states evolved. All the individuals in the population kept the configuration of the 3-bit DAC cells, two OpAmps cells and the two faulty cells. The response of the recovered circuit, achieved after about 30 generations, is shown in Figure 5.

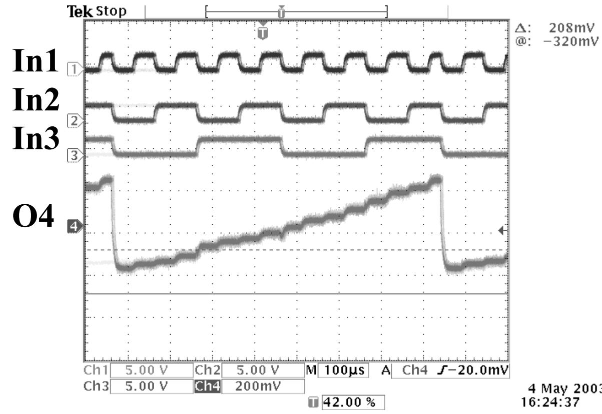

Figure 5. Recovered 4-bit DAC.

The originally evolved DAC had a fitness of 8.5. After the faults are applied, the fitness deteriorates (increases) to around 24. The best (recovered) individual found had a fitness of 3, superior to the originally evolved circuit. The recovery results were very consistent throughout different evolutionary runs, with good recovered DACs being achieved in almost all the runs.

It can be verified that recovered solution has a higher performance in terms of linearity comparing to the originally evolved 4-bit DAC. One possible reason is that a larger number of evolutionary runs was performed to recover the DAC than to evolve the original circuit. A second possible reason is that human designed OpAmps may not have been a good choice of building blocks for DAC evolution.

Let us now characterize the recovered solution. This circuit operates at Vdd equal to 2V. The digital inputs also have a 2V level. One performance criteria for DACs is the Differential Nonlinearity (DNL) [15]. This statistics is defined as:

DNL_i = Incremental height of transition i – Ideal Increment Height

In this particular case, there are 15 transitions, hence 15 different DNL values. The ideal voltage increment of each transition is equal to the voltage value of the LSB (Least Significant Bit) of the data converter, which is around 28mV in this case[1]. Therefore, according to the above equation, the ideal value of the DNL should be 0. Table 1 shows the 16 output voltages of the evolved DAC as well as the 15 DNL values.

[1] 1LSB = Vref/16, for Vref=453mV.

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Table 1. Output and on-linearity of recovered DAC.

Input (binary)	Output(mV)	DNL (LSB)
0000	160	---------------
0001	180	-0.29
0010	196	-0.43
0011	220	-0.14
0100	264	0.57
0101	288	-0.14
0110	308	-0.29
0111	336	0
1000	364	0
1001	396	0.14
1010	412	-0.42
1011	440	0
1100	480	0.43
1101	520	0.43
1110	556	0.29
1111	584	0

The DNL for the entire converter is 0.57LSB, since the overall error of the DAC is defined by the worst-case DNL. It is a common practice to assume that a converter with N-bit resolution will have less than ± 0.5LSB DNL.

6. Conclusions

These experiments demonstrated the evolutionary recovery applied to a larger circuit than experiments previously reported. In this case the faults were applied to entire FPTA cells as opposed to only some components inside the cell. Self-recovery has been performed consistently and in a very smaller fraction of time (less than a minute) comparing to other experiments in the literature. It has also been observed that a 4-bit DAC with good linearity could be evolved using SABLES. Next experiments will involve increasing the DAC resolution to 5 or 6 bits and investigating evolutionary recovery when faults are applied to more cells.

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